Numerical and Experimental Exploration of Thermal Isolation in 3D Systems Using Air Gap and Mechanically Flexible Interconnects

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ABSTRACT

This paper proposes a thermal isolation technology using air gap and mechanically flexible interconnects (MFIs) for heterogeneous 3-D integration. Thermal modeling shows that the proposed architecture achieves a temperature reduction of approximately 40.0% in the low-power tier compared to conventional approaches using microbumps and underfill. To demonstrate the technology, a two-tier testbed is fabricated, assembled and tested. The experimental results of test cases show an average temperature reduction of approximately 30.0% in the low-power tier.

I. INTRODUCTION

One of the key thermal challenges for three dimensional (3D) integrated circuits (ICs) is thermal coupling between tiers. In heterogeneous integration such as memory-on-logic and logic-on-silicon photonics, a thermal isolation solution may be necessary to 'protect' the low-power tier from the transient thermal variation and coupling of the high-power tier [1] [2].

For instance, in a DRAM-processor stack, the stacked DRAM will experience an elevated temperature [3]; higher DRAM junction temperature (approximately 90 °C~100 °C) degrades memory performance by 8.6% and results in 16.1% additional power consumption [4]. Likewise, in silicon nanophotonics, microring resonators are highly sensitive to temperature variations, and thus complex stabilizer circuits and dense heaters are used to compensate for this thermal variation [5]. With a temperature drift of 8 ºC, the tuning power is as high as 0.19 nJ/bit (26.7% of total communication power) [6] and will increase under a higher temperature drift. Therefore, in order to maintain system performance and increase power efficiency, there is an urgent call for novel technologies to reduce the thermal crosstalk for these heterogeneous 3D stacks to 'protect' the low-power and temperature sensitive tiers.

In most state-of-art 3D approaches, tiers are bonded using microbumps along with underfill, which is applied between tiers to reduce the thermomechanical stress on the solder microbumps. However, the thermal conductivity of underfill is approximately 0.4 W/m·K ~ 5 W/m·K. This will introduce a small thermal resistance between the two tiers and hence cause thermal coupling between the tiers.

Integrating an air gap between tiers in 3D ICs was proposed as a solution to thermally decouple a temperature sensitive tier [2][7]. It is shown that by integrating an air gap layer between the memory and logic, the temperature of the memory tier can be reduced by 25.7 °C [2]. However, the proposed approach did not address thermomechanical challenges nor reported experimental results of the thermal isolation approach. Therefore, we propose to integrate an air gap and mechanically flexible interconnects (MFIs) [8] to replace both the microbumps and the underfill. The proposed 3D IC approach is shown in Fig. 1. Unlike rigid solder microbumps, MFIs can deform elastically under stress, which helps maintain reliable electrical connectivity between tiers, thus eliminating the underfill and reducing the thermal coupling between tiers.

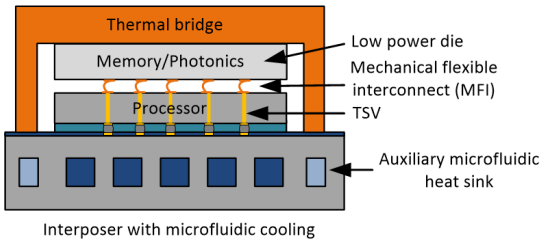

Fig. 1. Illustration of a heterogeneous 3-D IC application with MFIs and air gap.

The goal of this work is to numerically and experimentally explore the thermal isolation technology using MFIs and an air gap. We firstly use a compact thermal model to characterize and compare the proposed architecture with conventional solutions of microbump and underfill. With the guidance of the simulation results, a two-tier stack testbed [9] is designed, fabricated, and tested to emulate a stack of low-power and high-power tiers.

II. NUMERICAL EXPLORATION OF PROPOSED THERMAL ISOLATION TECHNOLOGY

In this section, a finite-volume based thermal model [2] is used to thermally compare conventional 3-D stacks using underfill and microbumps to our proposed approach in Fig 1. The isolation technology consists of three components. First, the MFIs and air gap provide thermal isolation between tiers. Second, there are two separate interposer embedded microfluidic heat sinks (MFHS): the central MFHS is for removing the heat from the high-power tier and the auxiliary MFHS is for removing the heat from the top tier. Last, an extended heat spreader, thermal bridge is attached to the top tier as a designated heat path. Fig. 2(a) shows a simplified configuration of our proposed architecture where the thermal

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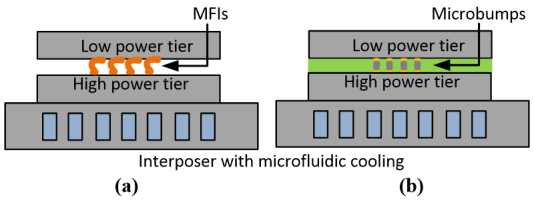

Fig. 2. Modeled stack with (a) isolation technology using MFIs and air gap (b) conventional 3-D stack using microbumps and underfill

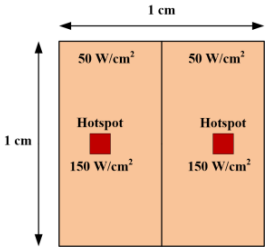

Fig. 3. Power map of the bottom high-power die

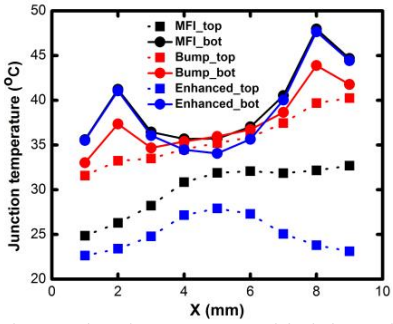

Fig. 4. Thermal comparison between proposed isolation and conventional technologies

bridge is removed to reduce the fabrication complexity. Fig 2(b) shows a benchmark stack using microbumps and underfill.

Fig 3 shows the power map of the bottom tier, which consists of a 50 W/cm^2 of background heating with two hotspots of 150 W/cm^2. Each hotspot is 1 mm × 1 mm. Since the focus of the experiments is on how the temperature of the high-power tier (bottom) impacts the low-power tier (top), we assign a fixed power dissipation of 0.5 W to the low-power tier. The inlet temperature of the coolant is assumed to be 19.93 °C (which matches the experimental values reported later in the paper). The heat transfer coefficient for the bottom tier is assumed to be 5.2 × 10^4 W/m^2·K. The cooling of the thermal bridge is modeled as a convection coefficient of 1.3×10^4 W/m^2·K.

The simulation results are shown in Fig 4. For the case using microbumps and underfill (red curves), the temperature of the two tiers are almost identical, indicating significant thermal coupling. At the hotspot near the outlet port (right side), the temperature of the upper tier and the lower tier is 39.7 °C and 43.9 °C, respectively. For the case using thermal isolation (black curves), the temperature of the upper tier and the lower tier is 32.2 °C and 48.0 °C, respectively. The thermal isolation technology is shown to reduce the upper-tier temperature by 7.5 °C (18.9%) at the hotspot located at the right side. For the proposed architecture with an independent MFHS and thermal bridge, the temperature of low-power tier further drops. From Fig. 4 (blue curves), the temperature of the upper tier and the lower tier is 23.8 °C and 47.7 °C, respectively. A temperature

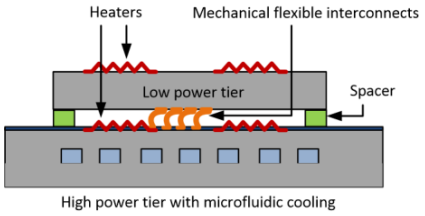

Fig. 5. Designed testbed for the evaluation of the proposed thermal isolation

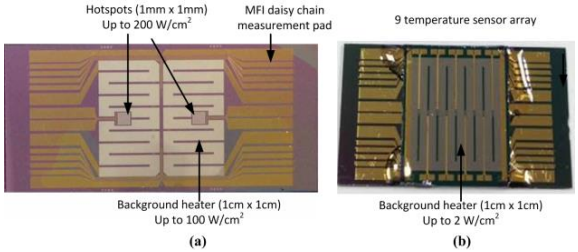

Fig. 6. Fabricated testbed (a) high-power (bottom) tier with two hotspots (b) assembled two-tier testbed with 9 temperature sensors

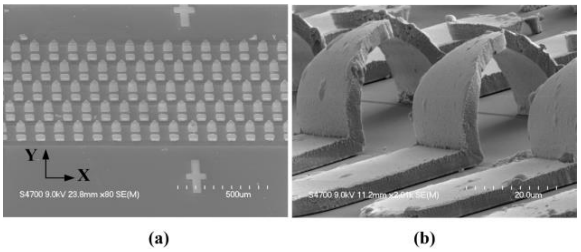

Fig. 7. SEM images of fabricated MFI array (a) top view (b) side view

reduction of 15.9 °C (40.0%) in the low-power tier is achieved compared to the case using microbumps and underfill (39.7 °C).

III. DESIGN OF THE TESTBED

Fig 5 shows the schematic of the testbed fabricated to experimentally evaluate thermal isolation. In the testbed, a microfluidic heat sink (MFHS) is integrated in the high-power tier (bottom tier). MFIs are used as interconnects between the two tiers (instead of microbumps) and designed to be clustered in the middle region to further enhance thermal isolation.

Fig. 6(a) shows the fabricated high-power tier. The chip area is 1 cm × 1 cm. There are two 1 mm × 1 mm hotspots in the chip and both are located 1.5 mm away from the edges. Fig. 6(b) shows the fabricated low-power tier; a spiral heater is formed over the whole chip to generate a uniform power map. Nine resistance temperature detectors (RTDs) are integrated along the middle of the chip in order to measure the temperature across the low-power tier.

The MFI array contains 12 × 100 MFIs based on the wide I/O specifications [10]. The MFI design has a pitch of 75 µm × 100 µm (X, Y). Fig. 7(a) and (b) show the SEM images of the freestanding MFIs. The height of the MFIs is 25 µm. Four-point and daisy-chain resistance measurements of 38 MFIs are performed to verify the electrical connections of the MFIs throughout thermal testing.

The microfluidic test setup is similar to [1]. In all tests, the inlet deionized water temperature is 19.5 °C ± 0.5 °C. An Agilent DC power analyzer is used to source current into the on-chip

Table I Power assignment of the bottom tier

Case	Background (W/cm^2)	Hotspot (W/cm^2)
Initial	0	0
A	30	100
B	30	150
C	10	10
D	10	150

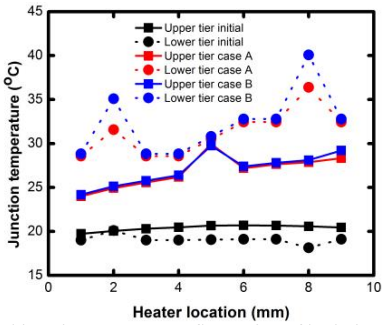

Fig. 8. Measured junction temperature fluctuation of both tiers in initial case, case A and case B.

heater/RTDs on both tiers. A data logger is used to measure the resistance of the RTDs on the top and bottom tiers to extract the junction temperatures.

IV. THERMAL EXPERIMENTAL RESULTS

Similar to the simulations above, we fix the low-power tier (top) to 0.5 W uniform background power dissipation and change the power map of high-power tier (bottom) to emulate different cases. The junction temperature at the center of the bottom tier is computed as the average of the left and right background temperatures. Except at the hotspots, all the other points of the bottom tier are plotted using the corresponding background temperature. The power value assignments of the high-power tier (bottom) are summarized in Table I. The power maps are similar to the one shown in Fig. 3 except the value for background and hotspot power.

A. Thermal testing I: Powering the high-power tier

In this experiment, there are three cases: initial case, case A, and case B listed in Table I. The junction temperature across the two tiers is shown in Fig. 8.

In the initial case, the temperature of both tiers is close to the inlet water temperature. When the bottom tier is powered to a background power density of 30 W/cm^2 and a hotspot power density of 100 W/cm^2 (case A), owing to the thermal isolation technology, the temperature of top tier (peak temperature: 24.9 °C and 27.9 °C) is not as high as the bottom tier (peak temperature: 31.6 °C and 36.4 °C). Moreover, the highest temperature in the upper tier is located at the center of the die (29.97 °C). This effect results from the fact that the dense MFIs are clustered in the middle and, thus, creating an enhanced thermal path. Even as the hotspot power is increased to 150 W/cm^2 in case B, we observe the temperature of the left and right hotspots in the upper die to increase to 35.1 °C and 40.1 °C, respectively while the bottom tier experiences virtually no temperature change (28.1 °C, 32.4% lower than the hotspot temperature).

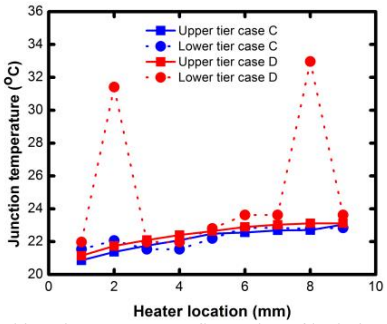

Fig. 9. Measured junction temperature fluctuation of both tiers in case C and case D.

B. Thermal testing II: Minimizing hotspot coupling

In this experiment, we investigate two additional power maps to further explore hotspot decoupling: case C and case D listed in Table I. The corresponding temperature of each case is shown in Fig. 9. In case C, the temperature curve is relatively flat indicating uniform temperature without hotspots. As the power density of the hotspot increases in case D, it is observed that there are two peak temperatures in the bottom die. The two peak temperatures are 31.4 °C and 33 °C, respectively. However, in case D, there are no obvious hotspots in the upper tier. The temperature of the upper tier gradually increases from 21.1 °C to 23.1 °C. This demonstrates that the proposed thermal isolation approach effectively minimizes hotspot coupling.

V. CONCLUSION

The paper proposes and demonstrates a thermal isolation technology using air gap and MFIs for heterogeneous 3-D integration. Various thermal tests are performed, and the experimental results show that the technology effectively decouples the two tiers thermally. The results of test cases show an average temperature reduction of approximately 30% in the low-power tier.

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